What is claimed is:

1. A non-volatile semiconductor memory device, comprising:

a memory cell array including a plurality of electrically erasable programmable non-volatile memory cells arrayed and divided into a plurality of blocks;

a plurality of word lines arranged in each of said plurality of blocks and each commonly connected to memory cells on an identical row;

a plurality of drive lines provided corresponding to said plurality of word lines and each arranged to supply a voltage to the corresponding word line;

a plurality of transfer transistors each operative as a switch to connect the corresponding word line to the corresponding drive line among said plurality of word lines and said plurality of drive lines,

wherein said plurality of word lines are classified into an arbitrary word line determined arbitrarily, secondary adjacent word lines located adjacent to both word lines adjacent to said arbitrary word line, and residual word lines other than said arbitrary word line and said secondary adjacent word lines, and

wherein among said plurality of transfer transistors, transfer transistors for said residual word lines are arranged at both adjacent locations and an opposite location around a transfer transistor for said arbitrary word line.

2. The non-volatile semiconductor memory device according to claim 1, further comprising a first device isolation insulator formed along an extending direction of a gate line for said plurality of transfer transistors,

wherein said plurality of transfer transistors each include a first impurity region connected to the corresponding word line among said plurality of word lines and a second impurity region connected to the corresponding

drive line among said plurality of drive lines,

wherein said plurality of transfer transistors are divided into a first group consisting of transfer transistors having said first impurity regions formed along said first device isolation insulator, and a second group consisting of transfer transistors having said first impurity regions formed as opposed to said first impurity regions of said first group via said first device isolation insulator, and

wherein said first impurity regions of said transfer transistors for said residual word lines are arranged at both adjacent locations and an opposite location around said first impurity region of said transfer transistor for said arbitrary word line.

3. The non-volatile semiconductor memory device according to claim 2, wherein said plurality of word lines each include a control gate of the corresponding memory cell among said plurality of memory cells, and a lead wire led out of said first impurity region of the corresponding transfer transistor among said plurality of transfer transistors and located on an upper layer above said control gate, and

wherein said control gates and said lead wires are arranged in the same order.

4. The non-volatile semiconductor memory device according to claim 2, wherein said plurality of word lines each include a control gate of the corresponding memory cell among said plurality of memory cells, and a lead wire led out of said first impurity region of the corresponding transfer transistor among said plurality of transfer transistors and located on an upper layer above said control gate, and

wherein said control gates and said lead wires are arranged in different orders.

5. The non-volatile semiconductor memory device according to claim 3, further comprising a multi-layered structure including a plurality of conductive layers and interlayer insulators interposed therebetween, wherein said lead wire is composed of a conductive layer disposed one-layer higher than said control gate among said plurality of conductive layers.

6. The non-volatile semiconductor memory device according to claim 4, further comprising a multi-layered structure including a plurality of conductive layers and interlayer insulators interposed therebetween, wherein said lead wire is composed of a conductive layer disposed one-layer higher than said control gate among said plurality of conductive layers.

7. The non-volatile semiconductor memory device according to claim 1, wherein among said plurality of transfer transistors, a transfer transistor for said residual word line is arranged at an obliquely opposite location around said transfer transistor for said arbitrary word line.

8. The non-volatile semiconductor memory device according to claim 1, wherein among said plurality of transfer transistors, transfer transistors for said residual word lines other than both word lines located adjacent to said arbitrary word line are arranged at both adjacent locations and an opposite location around said transfer transistor for said arbitrary word line.

9. The non-volatile semiconductor memory device according to claim 2, further comprising a second device isolation insulator formed along said extending direction of said gate line for said plurality of transfer

transistors and having a larger width compared to said first device isolation insulator,

wherein said plurality of transfer transistors are divided into a third group in addition to said first and second groups, said third group consisting of transfer transistors having said first impurity regions formed as opposed to said second impurity regions in said second group via said second device isolation insulator.

10. The non-volatile semiconductor memory device according to claim 1, said non-volatile semiconductor memory device comprises a NAND-type EEPROM.

11. An electronic card including said non-volatile semiconductor memory device according to claim 1 as mounted thereon.

12. An electronic device, comprising:

a card interface;

a card slot connected to said card interface; and

said electronic card according to claim 11 electrically connectable to said card slot.

13. The electronic device according to claim 12, wherein said electronic device comprises a digital camera.

14. A non-volatile semiconductor memory device, comprising:

a memory cell array including a plurality of electrically erasable programmable non-volatile memory cells arrayed and divided into a plurality of blocks;

a plurality of word lines arranged in each of said plurality of blocks and each commonly connected to memory cells on an identical row, and being classified into an arbitrary word line determined arbitrarily, secondary adjacent word lines located adjacent to both word lines

adjacent to said arbitrary word line, and residual word lines other than said arbitrary word line and said secondary adjacent word lines;

a plurality of drive lines provided corresponding to said plurality of word lines and each arranged to supply a voltage to the corresponding word line;

a plurality of transfer transistors each operative as a switch to connect the corresponding word line to the corresponding drive line among said plurality of word lines and said plurality of drive lines, and being arranged transfer transistors for said residual word lines at both adjacent locations and an opposite location around a transfer transistor for said arbitrary word line among said plurality of transfer transistors.